UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/627,993	07/28/2003	Eli Laufer	MRV-91321-860421	4250

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EXAMINER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

	Application No.	Applicant(s)
	10/627,993	LAUFER ET AL.
Office Action Summary	Examiner	Art Unit	
	Dady Chery	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _28 July 2003_.

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-62_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-62_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

        1.☐ Certified copies of the priority documents have been received.

        2.☐ Certified copies of the priority documents have been received in Application No. _____.

        3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set
> forth in section 102 of this title, if the differences between the subject matter sought to be patented and
> the prior art are such that the subject matter as a whole would have been obvious at the time the
> invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

2.   The factual inquiries set forth in *Graham* v. *John Deere Co.*, 383 U.S. 1, 148

USPQ 459 (1966), that are applied for establishing a background for determining

obviousness under 35 U.S.C. 103(a) are summarized as follows:

    1.   Determining the scope and contents of the prior art.
    2.   Ascertaining the differences between the prior art and the claims at issue.
    3.   Resolving the level of ordinary skill in the pertinent art.
    4.   Considering objective evidence present in the application indicating
            obviousness or nonobviousness.

3.   This application currently names joint inventors. In considering patentability of

the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation

under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g)

prior art under 35 U.S.C. 103(a).

4.   Claims 1- 62 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Hadzic et al. (US Application 2004/0062278, hereinafter Hadzic)

Regarding claim 1, Hadzic discloses *a transmission module* (Fig. 1) for

transmitting Time Division Multiplexed ("TDM") data over an Ethernet network (106)

comprising:

i) *a TDM data converter/encapsulator* (112) for *receiving TDM data from a*

source;

ii) *a synchronous clock signal*(110) *associated with said TDM data;*

iii) *a clock frequency multiplier* (108) *coupled to said TDM data converter/*

encapsulator;

iv) *a switch for receiving converted/encapsulated TDM data and for receiving a*

master clock signal; The switch is an inherent component of the network

v) *wherein said master clock signal is generated by said clock frequency*

multiplier, said master clock signal being related to said synchronous clock signal

associated with said TDM data (Page 5, [0056]) wherein said switch is coupled to both

a) *said TDM data converter/encapsulator* (112), and

b) *said clock frequency multiplier* (108).

Hadzic discloses a system that encapsulates a TDM data with a synchronous

clock signal and the transfer the TDM data with the clock signal over a network to a

second TDM network (Fig. 1, Page 5, [0054] - [0056]). This is same function as the

instant application.

Hadzic discloses the claimed invention except Hadzic uses a different design from the instant invention. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the structure of the invention discloses by Hadzic to make the present invention, since it has been held that rearranging parts of an invention involved only routine skill in the art. *In re Japikse*, 86 USPQ 70 (CCPA 1950).

Regarding claims 2, 9, 22, 23, 32, 40, Hadzic discloses *the transmission module of , wherein said switch comprises at least two ports, and wherein said master clock signal governs and synchronizes the timing of data transmissions from said switch* (Page 5, [0057]).

Regarding claims 3, 24, Hadzic discloses *the transmission module, wherein said clock frequency multiplier has an input frequency, an output frequency, and a frequency multiplication ratio which is the ratio of said input and output frequencies, and wherein said clock frequency multiplier is adapted and arranged such that said output frequency is a multiple of said input frequency* (Page 12, [0102]).

Regarding claims 4, 34, 42 Hadzic discloses *the transmission module, wherein said output frequency equals said master clock frequency* (Page 12. [0102]).

Regarding claims 5, 14,25,35,43, Hadzic discloses *the transmission , wherein one or more of said input frequency, said output frequency, and said frequency multiplication ratio are digitally programmable* (Page 6, [0062]).

Regarding claims 6 and 36, Hadzic discloses *a reception module* (Fig. 1, 116,

104) *for receiving converted/encapsulated Time Division Multiplexed ("TDM") data over*

an Ethernet network (106) *comprising:*

i) a switch for receiving said converted/encapsulated TDM data from said Ethernet

network over at least one Ethernet communications medium; The switch is an inherent

component of the network.

ii) a TDM decapsulator (116) *coupled to said switch;*

iii) a clock recovery phase locked loop ("PLL") for receiving a frequency, said PLL being

adapted to adjust a phase of said frequency to provide a phase-adjusted frequency

(Page 4, [0025]);

iv) a clock frequency divider coupled to said PLL for dividing said phase-adjusted

frequency to recover a TDM clock signal associated with said TDM data (Fig. 2, 212

and Page 6, [0060]).

Hadzic discloses a system that encapsulates a TDM data with a synchronous

clock signal and the transfer the TDM data with the clock signal over a network to a

decapsulator to a second TDM network (Fig. 1, Page 5, [0054] - [0056]). This is same

function as the instant application.

Hadzic discloses the claimed invention except Hadzic uses a different design

from the instant invention. It would have been obvious to one having ordinary skill in the

art at the time the invention was made to use the structure of the invention discloses by

Hadzic to make the present invention, since it has been held that rearranging parts of

an invention involved only routine skill in the art. *In re Japikse*, 86 USPQ 70 (CCPA

1950).

Regarding claims 7, 37, Hadzic discloses *the module, wherein said TDM*

decapsulator is a) coupled to said clock frequency divider, and b) adapted and arranged

to serialize said received converted/encapsulated TDM data by means of said

recovered TDM clock signal (Fig. 2, Page 6, [0061]).

Regarding claims 8, 26, 38, Hadzic discloses *the module, wherein said*

converted/encapsulated TDM data is received as Ethernet packets and said Ethernet

packets are converted into at least one TDM protocol data stream (Page 5, [0056]).

Regarding claim 10, Hadzic discloses *the module, further comprising ix) a master*

clock signal which is adapted and arranged to govern and synchronize the timing of

data received via said switch (Page 4, [0025]).

Regarding claims 11, 27, Hadzic discloses the *module wherein said clock*

recovery PLL extracts a high frequency clock signal from said received Ethernet data

and said extracted frequency clock signal equals the data bit rate of said received TDM

data (Page 4, [0025]).

Regarding claims 12, 28, 33, 41,Hadzic discloses *the module according to claim*

6, wherein said clock frequency divider has an input frequency, an output frequency,

and a frequency division ratio which is the ratio of said input and output frequencies,

and wherein said divider is adapted and arranged such that said output frequency is a fraction of said input frequency (Page 6, [0061]).

Regarding claim 13, Hadzic discloses the module, wherein said output frequency equals said received TDM clock signal (Page 6, [0061]).

Regarding claims 15, 45, 49 and 61, Hadzic discloses a system for communicating Time Division Multiplexed data over an Ethernet network, a transmission module (Fig. 1) for transmitting Time Division Multiplexed ("TDM") data over an Ethernet network (106) comprising:

i) a TDM data converter/encapsulator (112) for receiving TDM data from a source;

ii) a synchronous clock signal(110) associated with said TDM data;

iii) a clock frequency multiplier (108) coupled to said TDM data converter/ encapsulator;

iv) a switch for receiving converted/encapsulated TDM data and for receiving a master clock signal; The switch is an inherent component of the network

v) wherein said master clock signal is generated by said clock frequency multiplier, said master clock signal being related to said synchronous clock signal associated with said TDM data (Page 5, [0056]) wherein said switch is coupled to both

a) said TDM data converter/encapsulator (112), and

b) said clock frequency multiplier (108).

a TDM decapsulator (116) coupled to said switch;

a clock recovery phase locked loop ("PLL") for receiving a frequency, said PLL being

adapted to adjust a phase of said frequency to provide a phase-adjusted frequency

(Page 4, [0025]);

iv) a clock frequency divider coupled to said PLL for dividing said phase-adjusted

frequency to recover a TDM clock signal associated with said TDM data (Fig. 2, 212

and Page 6, [0060]).

Hadzic discloses a system that encapsulates a TDM data with a synchronous

clock signal and the transfer the TDM data with the clock signal over a network to a

second TDM network (Fig. 1, Page 5, [0054] - [0056]). This is same function as the

instant application.

Hadzic discloses the claimed invention except Hadzic uses a different design

from the instant invention. It would have been obvious to one having ordinary skill in the

art at the time the invention was made to use the structure of the invention discloses by

Hadzic to make the present invention, since it has been held that rearranging parts of

an invention involved only routine skill in the art. In re Japikse, 86 USPQ 70 (CCPA

1950).

Regarding claim 16, Hadzic discloses the system wherein said at least one

transmission module and said at least one reception module are located distant from

one another and are adapted and arranged to function as a first operational pair for communicating data in a first direction (Fig. 1).

Regarding claim 17, Hadzic discloses *the system o, further comprising a second reception module and a second transmission module, wherein said second transmission module and said second reception module are operationally adapted and arranged to function as a second operational pair, and wherein said first and second operational pairs are adapted and arranged to function as a bidirectional communications system for communicating in said first direction and in a second direction, said second direction being opposite said first direction* (Fig. 1, Page 5, [0054] –[0055]).

Regarding claims 18 -21, Hadzic discloses *the system, wherein said at least one transmission module and said second reception module are co-located with one another to comprise a first transceiver module* (Fig. 1, Page 5, [0054] –[0055]).

Regarding claim 29, Hadzic discloses *a method for transmitting Time Division Multiplexed ("TDM") data over an Ethernet network* (Fig. 1) *comprising the acts of*

i) receiving said TDM data and a synchronous clock associated with said TDM data from a source by means of a TDM data converter/encapsulator;

ii) generating a master clock signal related to said synchronous clock signal,

iii) packetizing said TDM data,

iv) forwarding said packetized data and said master clock signal to a switch; and

v) switching said packetized TDM data onto at least one Ethernet communications media of said Ethernet network. (Page 5, [0054] – [0056])

Regarding claim 30, Hadzic discloses *the method, wherein said master clock signal is generated by said clock frequency multiplier, and said master clock is related to said synchronous clock signal associated with said TDM data, and wherein said switching is effected by a switch which is coupled to both said TDM data converter/encapsulator, and to said clock frequency multiplier* (Fig. 2, Page 6, [0060] – [0061]).

Regarding claim 44. Hadzic discloses *a method for communicating Time Division Multiplexed data* (Fig. 1) *over an Ethernet network* (106), *said method comprising the act of*

I) providing at least two transceiver modules (112, 116), *and II) operationally coupling, adapting or arranging said at least two transceiver modules to effect communication there between* (Page 5, [0054] – [0056]).

46. The method of claim 44, comprising the further acts of III) providing more than two of said transceiver modules, and IV) operationally coupling, adapting or arranging said more than two transceiver modules to effect communication or among any two or more of said modules.

Regarding claims 47, 57, Hadzic discloses *a network* (Fig. 1) *comprising:*

A) *a first Ethernet network (102) and a second Ethernet network (104), wherein each of*

said Ethernet networks is adapted for bi-directional communications between a

transmission module and a reception module of each of said Ethernet networks,

B) *at least one wide area network (WAN) (106) adapted for long-distance bi-directional*

communications, said wide area network being interposed between said first and said

second Ethernet networks,

C) *a plurality of operational pairs of switches adapted for performing clock recovery*

functions and data transfer functions between pairs of Ethernet networks, wherein said

first Ethernet network and said second Ethernet network are adapted to communicate

with one another through said wide area network (Page 5, [0056]).

Hadzic discloses the claimed invention except Hadzic uses a different design

from the instant invention. It would have been obvious to one having ordinary skill in the

art at the time the invention was made to use the structure of the invention discloses by

Hadzic to make the present invention, since it has been held that rearranging parts of

an invention involved only routine skill in the art. *In re Japikse*, 86 USPQ 70 (CCPA

1950).

Regarding claim 48, Hadzic discloses *the network, wherein each of said first and*

second Ethernet networks comprises at least one transmission module, and at least one

reception module (Fig. 1, Page 5, [0054] – [0055]).

Regarding claim 50, Hadzic discloses *the network, wherein each of said*

operational pairs of switches is adapted and configured between one of said Ethernet

*networks and said WAN to function as a transceiver switch pair (*Fig. 1, Page 5, [0054] –

[0055]).

Regarding claim 51, Hadzic discloses *the network, wherein said at least one*

Ethernet reception module and said at least one Ethernet transmission module are

*adapted or configured to form a single operational transceiver module (*Fig. 1, Page 5,

[0054] – [0065]).

Regarding claims 52 and 58, Hadzic discloses *the network of claim 47, wherein a*

first pair of said plurality of operational pairs of switches is configured as a transmission

switch pair such that

i) a first switch of said transmission switch pair accepts encapsulated Ethernet data from

one of said at least two Ethernet networks for transmission to a second switch of said

transmission switch pair, and

ii) said second switch of said transmission switch pair transmits said encapsulated

Ethernet data and interfaces with said WAN to transmit said encapsulated Ethernet data

over said WAN to a second pair of said plurality of pairs of switches, and wherein said

second pair of said plurality of switches is configured as a reception switch pair such

that,

iii) a first switch of said reception switch pair receives said encapsulated Ethernet data

via said WAN, and

iv) a second switch of said reception switch pair receives said encapsulated Ethernet data from said first switch of said reception switch pair for forwarding and distribution over a second of said at least two Ethernet networks (Fig. 1, Page 5, [0054] –[0057]).

The pair of switch is an inherent feature of the pair of network (102 and 104).

Regarding claim 53, Hadzic discloses the network, further comprising a plurality of said Ethernet networks and a plurality of said operational switch pairs (Fig. 1 and Page 5, [0056]).

Regarding claim 54, Hadzic discloses the network of claim 47, further comprising at least one TDM network, wherein said TDM network is adapted and configured to communicate with at least one of said Ethernet networks (Fig.1 [0056]).

Regarding claims 55 and 60, Hadzic discloses the network of claim 52, wherein said first pair of said plurality of operational pairs of switches is configured both as a transmission switch pair and a reception switch pair to form a transceiver switch pair for bidirectional communications (Fig. 1, Page 5, [0054] –[0057]).

Regarding claim 56 and 59, Hadzic discloses the network of claim 55, wherein said operational pairs of switches are implemented to form an adapted network switch (Fig. 1, Page 5, [0054] – [0057]).

Regarding claim 62, Hadzic discloses an adapted network switch (Fig. 2)

comprising:

i) a system clock generator (226)

ii) a control (224), processing and data switching matrix coupled to memory, said

control, processing and data switching matrix further coupled to said system clock

generator ;

iii) a plurality of data communication ports (Fig. 17) coupled to said system clock

generator, each of said ports further coupled to said control, processing and data

switching matrix via bidirectional data signals (Page 19, [00164], lines 21 -30); Where

the microprocessor (1735) performed TDM packetization and multiplexing among T1

ports and also ran the remaining parts of the system discloses by Hadzic.

iv) a clock switching matrix (Fig. 2,226,214)coupled to said control, processing

and data switching matrix via a control signal, said clock switching matrix configured

such that a clock used in transmitting data from said adapted network switch is the clock

recovered from the data when said data was received at said data communications port.

Hadzic discloses the claimed invention except Hadzic uses a different design

from the instant invention. It would have been obvious to one having ordinary skill in the

art at the time the invention was made to use the structure of the invention discloses by

Hadzic to make the present invention, since it has been held that rearranging parts of

an invention involved only routine skill in the art. *In re Japikse*, 86 USPQ 70 (CCPA

1950).

Conclusion

5.   The prior art made of record and not relied upon is considered pertinent to

applicant's disclosure. Buchholz (US Patent 5,239,545) discloses a channel access

control in a communication system.

6.   Petch et al. (US Application 2002/0001299) discloses a method and apparatus

for synchronization in a wireless network.

7.   Russell et al. (US Patent 6,496,519) Discloses a frame based data transmission

over synchronous digital hierarchy network.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Dady Chery whose telephone number is 571-270-1207.

The examiner can normally be reached on Monday - Thursday 8 am - 4 pm ESt.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Ricky Q. Ngo can be reached on 571-272-3139. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR.

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For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dady Chery 12/04/2007
8.

RICKY Q. NGO
SUPERVISORY PATENT EXAMINER